Enhancing Functional Debug Capabilities using ALLSCAN Test Structures

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Background

- **Functional debug**: Critical phase during post-Silicon hardware bringup and post-Silicon Validation
- **Challenge**: Using functional patterns to debug chip/ system operation
  - Insufficient observability
  - Time consuming
  - Difficulty in determining the right stimulus for targeted tests
  - State of the output ports : No significant information on state of the system needed to understand possible cause for system malfunction

Implementation Details

- **Mode of Operation**
  - **Functional Mode :** When system malfunctions and the need for debug arises
  - **Clock Halt Mode** : All the clocks of the design should be halted. Implemented with 1149 JTAG instruction
  - **ALLSCAN Mode** : All the flops are connected in single / multiple chain/s between TDI to TDO
    - Implemented with Single or Multiple 1149 JTAG instructions based on number of ALLSCAN chains
- Other **structures**
  - 1149 : Change mode of operation from functional to ALLSCAN
  - JTAG clock : Shift data through the ALLSCAN chain
- The order of execution for debug will be :
  Functional → Clock Halt → ALLSCAN

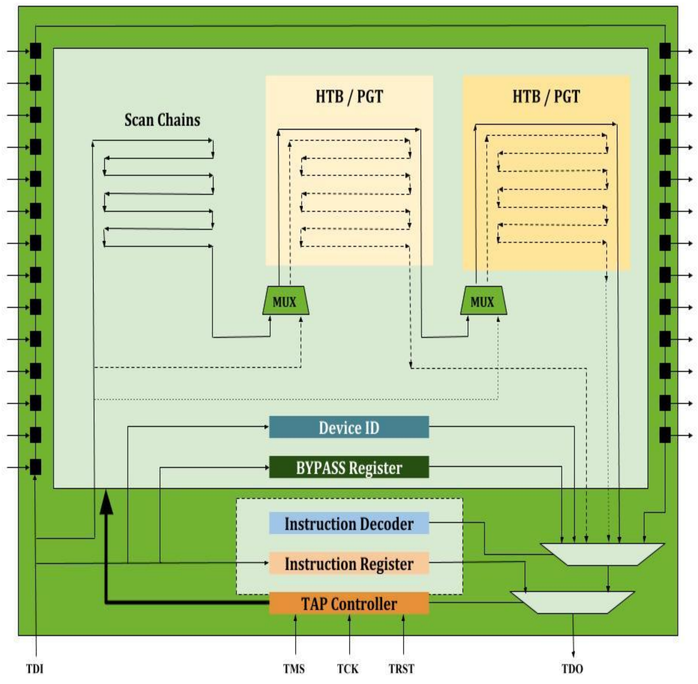
Proposed Architecture

- **ALLSCAN Mode**: All flops of the design are put into scan chain/s and made accessible through 1149 TAP
- Architecture solutions for ALLSCAN implementation
  - **Single ALLSCAN chain**: All flops of the design are cascaded to form one single scan chain
  - **Multiple ALLSCAN chains**: Multiple chains are created for different blocks of the design *(This approach is more meaningful for larger designs or hierarchically partitioned design, where it is convenient to observe a few flops at a time)*
- **At system malfunction**
  - **Switch the chip to manufacturing test mode**
  - **Scan out state of every flop in the design through manufacturing test scan out or 1149 JTAG ports using ALLSCAN Mode settings**

Execution Challenges

- **No commercial EDA tools** available to enable end-to-end solution
- Solution impacts architectural, implementation, verification aspects of the chip
  - **Implementation** : Needs architecture **planning**
    - Additional effort for structure insertion
  - **Validation**:
    - 1149 validation is impossible due to long scan chains
    - Serial simulations not feasible due to long run time
    - Verify using custom testbench
  - Impacts PD & Timing iterations & TAT

Structure



Functional Debug Use Case

- **Design A (Hardware verified)** :
  - **16.3M** Flops in single ALLSCAN chain
  - 128 Bit Electronic Chip ID was verified using ALLSCAN on hardware
  - 512 bits of functional TDRs verified using ALLSCAN on hardware
- **Design B (Hardware in few months)**:
  - **~34M** Flops in multiple ALLSCAN chains
  - All chains integrity verified through structural verification and simulations
  - 512 bits of functional TDRs verified using ALLSCAN through simulations